

Exhibit 9

Malikie Innovations Ltd. and Key Patent Innovations Ltd. v. Sophos Ltd.

Exhibit 9 – U.S. Patent No. 8,583,980

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Claims	Identification
[31pre] A device comprising:	<p>To the extent the preamble is limiting, Sophos devices implement LDPC, including a method of operating a transceiver comprising the steps below.</p> <p>Products sold/operated by Sophos that, on information and belief, support 802.11 with LDPC include:</p> <ul style="list-style-type: none"> • AP6 420/E/X • AP6 840/E • APX 120 • APX 320/X • APX 530 • APX 740 • XGS 87w • XGS 107w • XGS 116w • XGS 126w • XGS 136w • APX 740 • APX 320 • 7933DMC • AP55


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<p>[31a] a low-density parity-check (LDPC) encoder configured to:</p>	<p>Sophos devices (e.g., WiFi Access Points implement LDPC via Qualcomm WiFi Chipsets. For example, the AP 55 uses the Qualcomm QCA 9880. The APX 740 uses the Qualcomm IPQ8069</p> <div data-bbox="1131 456 1434 683" data-label="Image"> </div> <p>Qualcomm QCA9880</p> <p>Features</p> <ul style="list-style-type: none"> •WLAN CPU supports low-level setup of PHY and RF to offload the host processor for other tasks •Dynamic frequency selection (DFS) in required 5-GHz bands when used as an AP •3x3 MIMO technology improves effective throughput and range over existing 802.11a/b/g products •Supports spatial multiplexing, cyclic-delay diversity (CDD), <u>low-density parity check (LDPC)</u>, maximal ratio combining (MRC), Space Time Block Code (STBC) <p>https://www.qualcomm.com/products/internet-of-things/networking/wi-fi-networks/qca9880</p> <p>https://fccid.io/2ACTO-AP55/Internal-Photos/Internal-Photos-2586106</p>

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	<p>Sophos devices (e.g., WiFi Access Points implement LDPC via Qualcomm WiFi Chipsets. For example, the WiFi expansion module 7933DMC uses the Qualcomm QCA 9882</p>  <p>https://fcc.report/FCC-ID/2ACTO-7933DMC/6148568.pdf</p> <p>Product Highlights - KEY FEATURES</p> <ul style="list-style-type: none"> • <u>Qualcomm Atheros QCA9882</u> • 2.4GHz max 21dBm & 5GHz max 20dBm output power (per chain) • IEEE 802.11ac compliant & backward compatible with 802.11a/b/g/n • 2x2 MIMO Technology, up to 867Mbps • Mini PCI Express edge connector • Supports Spatial Multiplexing, Cyclic-Delay Diversity (CDD), <u>Low-Density Parity Check (LDPC) Codes</u>, Maximal Ratio Combining (MRC), Space Time Block Code (STBC) <p>https://www.524wifi.com/index.php/wle600vx-7a-minipcie-qca9882-module-802-11ac-2-2-2-4-5ghz-compex.html</p>

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	<p>Sophos devices (e.g., WiFi Access Points) implement LDPC. For example, AP6 access point transmits a beacon indicating support for LDPC</p> <p>Tag: SSID parameter set: "Sophos AP6 840 94172A_2"</p> <p>HT Capabilities Info: 0x098d</p> <p>....1 = HT LDPC coding capability: <u>Transmitter supports receiving LDPC coded packets</u></p> <p>Source: Wireshark PCAP file for AP6 Serial No. PC1005PC2DT28CO MAC address:</p>

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	<p>IEEE Std 802.11-2020</p> <p>IEEE Standard for Information Technology— Telecommunications and Information Exchange between Systems Local and Metropolitan Area Networks— Specific Requirements</p> <p>Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications</p> <p>4.3.13 High-throughput (HT) STA</p> <p>An HT STA has PHY features consisting of the modulation and coding scheme (MCS) set described in 19.3.5 and physical layer (PHY) protocol data unit (PPDU) formats described in 19.1.4. Some PHY features that distinguish an HT STA from a non-HT STA are referred to as multiple input, multiple output (MIMO) operation; spatial multiplexing (SM); spatial mapping (including transmit beamforming); space-time block coding (STBC); low-density parity check (LDPC) encoding; and antenna selection (ASEL)</p>

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<p>[31b] encode data using the following expanded parity check matrix:</p>	<p>IEEE Std 802.11-2020</p> <p>19.3.11.7.5 LDPC PPDU encoding process</p> <p>To encode an LDPC PPDU, step a) to step g) shall be performed in sequence:</p> <p>c) Compute the number of shortening bits, N_{shrt}, to be padded to the N_{pld} data bits before encoding, as shown in Equation (19-37).</p> <p>For all values of N_{shrt}, encode each of the codewords using the LDPC encoding technique described in 19.3.11.7.2 to 19.3.11.7.4. When , the shortened bits shall be discarded after encoding.</p>

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	<p>IEEE Std 802.11-2020</p> <p>19.3.11.7.3 LDPC encoder</p> <p>For each of the three available codeword block lengths, the LDPC encoder supports rate 1/2, rate 2/3, rate 3/4, and rate 5/6 encoding. The LDPC encoder is systematic, i.e., it encodes an information block, $c=(i_0, i_1, \dots, i_{(k-1)})$, of size k, into a codeword, c, of size n, $c=(i_0, i_1, \dots, i_{(k-1)}, p_0, p_1, \dots, p_{(n-k-1)})$, by adding $n-k$ parity bits obtained so that $H \times c^T = 0$, where H is an $(n-k) \times n$ parity-check matrix. The selection of the codeword block length (n) is achieved via the LDPC PPDU encoding process described in 19.3.11.7.5.</p>

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	<div>IEEE Std 802.11-2020</div> <div>Annex F</div> <div>(normative)</div> <div>HT LDPC matrix definitions</div> <div>Table F-3 defines the matrix prototypes of the parity-check matrices for a codeword block length $n = 1944$ bits, with a subblock size $Z = 81$ bits.</div> <div><div>(b) Coding rate $R = 2/3$.</div><table><tr><td>61</td><td>75</td><td>4</td><td>63</td><td>56</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>8</td><td>-</td><td>2</td><td>17</td><td>25</td><td>1</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>56</td><td>74</td><td>77</td><td>20</td><td>-</td><td>-</td><td>-</td><td>64</td><td>24</td><td>4</td><td>67</td><td>-</td><td>7</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>28</td><td>21</td><td>68</td><td>10</td><td>7</td><td>14</td><td>65</td><td>-</td><td>-</td><td>-</td><td>23</td><td>-</td><td>-</td><td>-</td><td>75</td><td>-</td><td>-</td><td>0</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td></tr><tr><td>48</td><td>38</td><td>43</td><td>78</td><td>76</td><td>-</td><td>-</td><td>-</td><td>-</td><td>5</td><td>36</td><td>-</td><td>15</td><td>72</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>-</td><td>-</td><td>-</td></tr><tr><td>40</td><td>2</td><td>53</td><td>25</td><td>-</td><td>52</td><td>62</td><td>-</td><td>20</td><td>-</td><td>-</td><td>44</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>-</td><td>-</td><td>0</td><td>0</td><td>-</td><td>-</td></tr><tr><td>69</td><td>23</td><td>64</td><td>10</td><td>22</td><td>-</td><td>21</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>68</td><td>23</td><td>29</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td><td>-</td></tr><tr><td>12</td><td>0</td><td>68</td><td>20</td><td>55</td><td>61</td><td>-</td><td>40</td><td>-</td><td>-</td><td>-</td><td>52</td><td>-</td><td>-</td><td>-</td><td>44</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>0</td></tr><tr><td>58</td><td>8</td><td>34</td><td>64</td><td>78</td><td>-</td><td>-</td><td>11</td><td>78</td><td>24</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>58</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td></tr></table></div>	61	75	4	63	56	-	-	-	-	-	8	-	2	17	25	1	0	-	-	-	-	-	-	56	74	77	20	-	-	-	64	24	4	67	-	7	-	-	-	0	0	-	-	-	-	-	28	21	68	10	7	14	65	-	-	-	23	-	-	-	75	-	-	0	0	-	-	-	-	48	38	43	78	76	-	-	-	-	5	36	-	15	72	-	-	-	-	0	0	-	-	-	40	2	53	25	-	52	62	-	20	-	-	44	-	-	-	-	0	-	-	0	0	-	-	69	23	64	10	22	-	21	-	-	-	-	-	68	23	29	-	-	-	-	-	0	0	-	12	0	68	20	55	61	-	40	-	-	-	52	-	-	-	44	-	-	-	-	-	0	0	58	8	34	64	78	-	-	11	78	24	-	-	-	-	-	58	1	-	-	-	-	-	0
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<p>[31c] wherein -1 represents an 81x81 all-zero square matrix, and any other integer, s_{ij}, represents an 81x81 identity matrix circularly right shifted by a shift amount equal to s_{ij}.</p>	<p>IEEE Std 802.11-2020</p> <p>19.3.11.7.4 Parity-check matrices</p> <p>Each of the parity-check matrices is partitioned into square subblocks (submatrices) of size $Z \times Z$. These submatrices are either cyclic-permutations of the identity matrix or null submatrices.</p> <p>The cyclic-permutation matrix P_i is obtained from the $Z \times Z$ identity matrix by cyclically shifting the columns to the right by i elements. The matrix P_0 is the $Z \times Z$ identity matrix. Figure 19-12 illustrates examples (for a subblock size of 8×8) of cyclic-permutation matrices P_i.</p> <p>Table F-1 displays the “matrix prototypes” of parity-check matrices for all four coding rates at block length $n=648$ bits. The integer i denotes the cyclic-permutation matrix P_i, as illustrated in Figure 19-12. Vacant entries of the table denote null (zero) submatrices.</p> <p>Table F-2 displays the matrix prototypes of parity-check matrices for block length $n=1296$ bits, in the same fashion.</p> <p>Table F-3 displays the matrix prototypes of parity-check matrices for block length $n=1944$ bits, in the same fashion.</p>

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